

| | |
|----------------|---------------------------------------|
| 03-IBVP | Advanced Computer Architecture |
|----------------|---------------------------------------|

Lehrform (*teaching format*) / **SWS** (*hours per week*): 2VL + 2UE

Kreditpunkte (*credit points*): 6

Turnus (*frequency*): usually, each summer term

Inhaltliche Voraussetzungen (*content-related prior knowledge/skills*): Computer Architecture and Embedded Systems

Sprache (*language*): English

Lehrende (*teaching staff*): AG Rechnerarchitektur (Prof. Dr. Rolf Drechsler)

| Studiengang (<i>degree program</i>) | Module | Semester |
|--|--------------------------------------|-----------------|
| Informatik (Bachelor VF) | IBVP | ab 4.Sem. |
| Systems Engineering (Bachelor) | V07-ESS-V | ab 4.Sem. |
| Informatik (Master) | <i>General Studies</i> | ab 1.Sem. |
| Systems Engineering I/II (Master) | M07-AM-INF | ab 1.Sem. |
| (<i>weitere SGe</i>) | <i>General Studies / Free Choice</i> | ab 1. Sem. |

Lernergebnisse / *Learning Outcome*:

- Students have an extensive knowledge on various specific topics of computer architecture
- Students understand instruction pipeline concepts and instruction level parallelism
- Students have an understanding multi-core systems and graphic processing units.
- Students have an understanding of cache design and cache coherency algorithms
- Students are capable of applying the introduced topics with the help of RISC-V

Inhalte / *Contents*:

This course focuses on advanced concepts of computer architecture. The students will be introduced with advanced aspects of processor design with special emphasis on instruction pipeline concepts and compiler techniques for enhancing instruction level parallelism (ILP). Other architectural aspects like superscalar and very large instruction word (VLIW) architectures, and also systolic array and other data-driven architectures will also be discussed. Concepts of multi-core systems and graphic processing units (GPUs) will also be covered. Furthermore, cache design for optimizing processor-memory bandwidth, and various cache coherency algorithms will be discussed in the context of multi-processor systems. Finally the course will introduce some domain specific architectures and some emerging in-memory computing architectures. The processor concepts and other aspects of architecture will be guided by RISC-V as a case study.

Hinweise (*remarks*): The table lists only the primary / most specific modules to which this course is assigned.