03-IMVP-DLS	Digital Logic Synthesis

Lehrform *(teaching format)* / **SWS** *(hours per week)*: 2VL + 2UE

Kreditpunkte *(credit points)*: 6

Turnus *(frequency)*: usually, each winter term

Inhaltliche Voraussetzungen *(content-related prior knowledge/skills)*: NONE

Sprache *(language)*: English

Lehrende *(teaching staff)*: AG Rechnerarchitektur (Prof. Dr. Rolf Drechsler)

Studiengang *(degree program)*	Module	Semester
Informatik (Master)	IMVP, IMVP-SQ	ab 1.Sem.
Systems Engineering I/II (Master)	M07-VT-ESS?	ab 1.Sem.
Informatik (Bachelor VF)	(nur *Freie Wahl*)	ab 4.Sem.

Lernergebnisse / *Learning Outcome*:

- Understand and have the ability to explain the synthesis process from different abstraction levels
- Understand the importance and usefulness of abstraction
- Understand the automation techniques for the synthesis process
- Understand and have the ability to explain different optimization techniques for digital logic synthesis
- Have the ability to assign different optimization techniques to different abstraction levels in synthesis

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Inhalte / *Contents*:

In this course the students are going to be introduced to the methods used for Digital Logic Synthesis, i.e., to take the design represented at various levels of abstraction down to basic digital gates. The key aspect of this course is to make them aware of the usefulness of abstraction in digital logic synthesis and to optimize the digital circuit for the given set of constraints.

This will enable students to not only understand the state of the art optimization techniques but the learning from this course can be used in emerging domains for efficient logic synthesis. Given the complexity of the digital systems in the modern world, automation is key in making the problem of digital logic synthesis feasible. The basic intuition behind optimization will be developed using linear programming and integer linear programming.

The first optimization will be at the architectural level. The study at this level deals with capturing the behavior from a macroscopic viewpoint represented in the form of data flow graphs. The optimization of these graphs in terms of resource and time constraints will be done. Scheduling and Binding will be discussed at depth to perform optimizations at the architectural level. Next, we will move at the lower level of abstraction, logic level. The basics of Boolean logic representation and manipulation for digital logic synthesis will be discussed.

The next part of the course deals with the two level logic minimization. We will discuss in brief about the Exact minimization algorithms but will discuss in detail about the heuristic based methods for two level logic optimization. Lastly, we will discuss the multilevel logic optimization techniques.

Module overview:

- Introduction to Optimization
- Architectural Synthesis
- Boolean Algebra
- Heuristics-based Optimization
- Multilevel Logic Minimization

Hinweise *(remarks)*: The table lists only the primary / most specific modules to which this course is assigned.