03-IMVP-RTL	Register Transfer Level (RTL) Digital Systems Modeling with Verilog HDL

Lehrform *(teaching format)* / **SWS** *(hours per week)*: 2VL + 2UE

Kreditpunkte *(credit points)*: 6

Turnus *(frequency)*: i.d.R. jedes SoSe

Inhaltliche Voraussetzungen *(content-related prior knowledge/skills)*: KEINE

Sprache *(language)*: English

Lehrende *(teaching staff)*: AG Rechnerarchitektur (Prof. Dr. Rolf Drechsler)

Studiengang *(degree program)*	Module	Semester
Informatik (Master)	IMVP, IMVP-SQ	ab 1.Sem.
Systems Engineering I/II (Master)	M07-VT-ESS	ab 1./2.Sem.
Informatik (Bachelor VF)	(nur *Freie Wahl*)	ab 4.Sem.

Lernergebnisse/*Learning Outcome*:

- Students understand the core principles of Verilog and are familiar with its syntax
- Students are capable of describing Hardware with Verilog
- Students are introduced to sequential circuits and know the influence of clock gating, pipelining and memories
- Students understand the composition of circuits into datapaths and controllers with several examples
- Students are familiar with Static Timing Analysis and how to apply this to circuits with timing violations

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Inhalte/*Contents*:

In this course the student is introduced to digital design on register transfer layer (RTL) with Verilog as a hardware description language (HDL). Initially different layers of abstraction (around RTL) and different HDLs are compared. Along known combinatorial logic the student is introduced to Verilog's language concepts (syntax and semantics to describe circuits). The typical operators of Verilog and available primitives (used but not as often) are introduced to describe typical (known) combinatorial circuits (multiplexer, adders, etc.). Alongside known circuits the students are instructed about the pitfalls of describing hardware vs programming software and are given a set of guidelines on how to write/describe digital hardware circuits (so they become synthesizable in real hardware). After that sequential circuits are the next topic, which is introduced through the most basic building block, the flipflop. Bigger building blocks of sequential circuits are introduced and their Verilog description is walked through. The used techniques are discussed with additional techniques of digital design (clock gating, pipelining, memories). The main part of the course starts with the RTL point of view. The decomposition of every circuit into a Datapath and a controller is shown on various examples. The goal is to show how various data paths and controllers can look like and how they are designed. There is an additional section for practical topics of digital design: Static Timing Analysis and how to solve problems occurring in circuits with timing violations. For the last two parts of the course at first communication mechanisms for digital systems are discussed, at last a medium/intermediate level example is given with a RISC-V RV32I processor.

Hinweise *(remarks)*: In der Tabelle sind nur die primären/spezifischsten Module aufgelistet, denen diese Veranstaltung zugeordnet ist.